What is claimed as new and desired to be protected by Letters Patent of the United States is:

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1. A charge pump circuit comprising:

a first plurality of serially connected transistors of a first conductivity type;

a second plurality of serially connected transistors of a second conductivity type;

said first plurality of serially connected transistors being serially connected to the second plurality of serially connected transistors;

the interconnection of said first and second plurality of transistors providing an output;

a gate of one of said first plurality of transistors being adapted to receive a $\overline{\text{DOWN}}$ pulse signal, a gate of another one of said first plurality of transistors being adapted to receive a DC bias signal, a gate of one of said second plurality of transistors being adapted to receive an UP

pulse signal, and a gate of the other of said second plurality of transistors being adapted to receive another DC bias signal; and

a first node at the interconnection of transistors of said first plurality of transistors being adapted to receive a $\overline{\text{DOWN}}$ pulse signal and a second node at the interconnection of transistors of said second plurality of transistors being adapted to receive an $\overline{\text{UP}}$ pulse signal.

2. A charge pump circuit as in claim 1 wherein said first plurality of transistors are p-channel transistors and said second plurality of transistors are n-channel transistors.

3. A charge pump circuit as in claim 1 further comprising a first capacitor circuit for coupling said DOWN pulse signal to said first node and a second capacitor circuit for coupling said $\overline{\text{UP}}$ pulse signal to said second node.

4. A charge pump circuit as in claim 1 wherein said first plurality of transistors is a pair of transistors and said second plurality of transistors is a pair of transistors.

5. A CMOS logic circuit comprising:

a first circuit portion containing transistors of a first conductivity type and a second circuit portion containing transistors of a second conductivity type, said first and second circuit portions being interconnected and the interconnection defining an output, said first circuit portion being responsive to first and second complementary pulse signals and a first DC bias signal, said second circuit portion being responsive to third and fourth complementary pulse signals and a second DC bias signal.

6. A CMOS logic circuit as in claim 5 further comprising a respective capacitor circuit for coupling said second and fourth complementary signals to said respective first and second circuit portions.

7. A CMOS switching circuit comprising:

a p-channel switching transistor, said p-channel switching transistor having a gate for receiving a first switching signal;

a p-channel bias transistor connected in series with said p-channel switching transistor, said p-channel bias transistor having a gate for receiving a bias voltage, said serially connected p-channel switching

transistor and p-channel bias transistor being connected between a first potential source and an output terminal;

an n-channel switching transistor, said n-channel switching transistor having a gate for receiving a second switching signal;

an n-channel bias transistor connected in series with said n-channel switching transistor, said n-channel bias transistor having a gate for receiving a bias voltage, said serially connected n-channel switching transistor and n-channel bias transistor being connected between said output terminal and a second potential source;

a first capacitor for coupling a complementary version of said first switching signal to a connection node of said p-channel transistors; and

a second capacitor for coupling a complementary version of said second switching signal to a connection node of said n-channel transistors.

8. A charge pump circuit comprising:

a first plurality of serially connected transistors of a first conductivity type;

a second plurality of serially connected transistors of a second conductivity type;

said first plurality of serially connected transistors being serially connected to the second plurality of serially connected transistors;

the interconnection of said first and second plurality of transistors providing an output;

a gate of one of said first plurality of transistors being adapted to receive a first switching signal, a gate of another one of said first plurality of transistors being adapted to receive a DC bias signal, a gate of one of said second plurality of transistors being adapted to receive a second switching signal, and a gate of the other of said second plurality of transistors being adapted to receive another DC bias signal; and

a first node at the interconnection of transistors of said first plurality of transistors being adapted to receive a complementary first switching signal and a second node at the interconnection of transistors of said second plurality of transistors being adapted to receive a complementary second switching signal.

9. A lock loop circuit comprising:

a voltage controlled oscillator;

a circuit for deriving a first clock signal from said voltage controlled oscillator;

a phase detector for receiving said first clock signal and a second clock signal, said phase detector producing first and second switching signals in accordance with a phase difference between said first and second clock signals;

a charge pump circuit for receiving said first and second switching signals and producing an output signal therefrom; and

a filter circuit receiving the output signal from said charge pump and providing a filtered signal to control said voltage control oscillator;

said charge pump circuit comprising:

a first plurality of serially connected transistors of a first conductivity type;

a second plurality of serially connected transistors of a second conductivity type;

said first plurality of serially connected transistors being serially connected to the second plurality of serially connected transistors;

the interconnection of said first and second plurality of transistors providing an output;

a gate of one of said first plurality of transistors being adapted to receive a first switching signal, a gate of another one of said first plurality of transistors being adapted to receive a DC bias

signal, a gate of one of said second plurality of transistors being adapted to receive a second switching signal, and a gate of the other of said second plurality of transistors being adapted to receive another DC bias signal; and

a first node at the interconnection of transistors of said first plurality of transistors being adapted to receive a complementary first switching signal and a second node at the interconnection of transistors of said second plurality of transistors being adapted to receive a complementary second switching signal.

10. A phase lock loop circuit as in claim 9 wherein said first plurality of transistors are p-channel transistors and said second plurality of transistors are n-channel transistors.

11. A phase lock loop as in claim 9 further comprising a first capacitor circuit for coupling said complementary first switching signal to said first node and a second capacitor circuit for coupling said complementary second switching signal to said second node.

12. A phase lock loop as in claim 9 wherein said first plurality of transistors is a pair of transistors and said second plurality of transistors is a pair of transistors.

13. A lock loop circuit comprising:

a voltage controlled oscillator;

a circuit for deriving a first clock signal from said voltage controlled oscillator;

a phase detector for receiving said first clock signal and a second clock signal, said phase detector producing first and second switching signals in accordance with a phase difference between said first and second clock signals;

a charge pump circuit for receiving said first and second switching signals and producing an output signal therefrom; and

a filter circuit receiving the output signal from said charge pump and providing a filtered signal to control said voltage control oscillator;

said charge pump circuit comprising:

a first circuit portion containing transistors of a first conductivity type and a second circuit portion containing transistors of a second conductivity type, said first and second circuit portions being interconnected and the interconnection defining an output, said first circuit portion being responsive to said first switching signal and its complement and a first DC bias signal, said second circuit portion being responsive to said second switching signal and its complement and a second DC bias signal.

14. A lock loop circuit as in claim 13 further comprising a respective capacitor circuit for coupling said first and second complementary signals to said respective first and second circuit portions.

15. A lock loop circuit comprising:

a voltage controlled oscillator;

a circuit for deriving a first clock signal from said voltage controlled oscillator;

a phase detector for receiving said first clock signal and a second clock signal, said phase detector producing first and second switching signals in accordance with a phase difference between said first and second clock signals;

a charge pump circuit for receiving said first and second switching signals and producing an output signal therefrom; and

a filter circuit receiving the output signal from said charge pump and providing a filtered signal to control said voltage control oscillator;

said charge pump circuit comprising:

a p-channel switching transistor, said p-channel switching transistor having a gate for receiving said first switching signal;

a p-channel bias transistor connected in series with said p-channel switching transistor, said p-channel bias transistor having a gate for receiving a bias voltage, said serially connected p-channel switching

transistor and p-channel bias transistor being connected between a first potential source and an output terminal;

an n-channel switching transistor, said n-channel switching transistor having a gate for receiving said second switching signal;

an n-channel bias transistor connected in series with said n-channel switching transistor, said n-channel bias transistor having a gate for receiving a bias voltage, said serially connected n-channel switching transistor and n-channel bias transistor being connected between said output terminal and a second potential source;

a first capacitor for coupling a complementary version of said first switching signal to a connection node of said p-channel transistors; and

a second capacitor for coupling a complementary version of said second switching signal to a connection node of said n-channel transistors.

16. A processor system comprising:

a processor; and

a data device coupled to said processor, at least one of said processor and data device including a charge pump circuit, said charge pump circuit comprising:

a first plurality of serially connected transistors of a first conductivity type;

a second plurality of serially connected transistors of a second conductivity type;

said first plurality of serially connected transistors being serially connected to the second plurality of serially connected transistors;

the interconnection of said first and second plurality of transistors providing an output;

a gate of one of said first plurality of transistors being adapted to receive a $\overline{\text{DOWN}}$ pulse signal, a gate of another one of said first plurality of transistors being adapted to receive a DC bias signal, a gate of one of said second plurality of transistors being adapted to receive an UP

pulse signal, and a gate of the other of said second plurality of transistors being adapted to receive another DC bias signal; and

a first node at the interconnection of transistors of said first plurality of transistors being adapted to receive a $\overline{\text{DOWN}}$ pulse signal and a second node at the interconnection of transistors of said second plurality of transistors being adapted to receive an $\overline{\text{UP}}$ pulse signal.

17. A processor system as in claim 16 wherein said first plurality of transistors are p-channel transistors and said second plurality of transistors are n-channel transistors.

18. A processor system as in claim 16 further comprising a first capacitor circuit for coupling said DOWN pulse signal to said first node and a second capacitor circuit for coupling said $\overline{\text{UP}}$ pulse signal to said second node.

19. A processor system as in claim 16 wherein said first plurality of transistors is a pair of transistors and second plurality of transistors is a pair of transistors.

20. A processor system comprising:

a processor; and

a data device coupled to said processor, at least one of said processor and data device including a charge pump circuit, said charge pump circuit comprising:

a first circuit portion containing transistors of a first conductivity type and a second circuit portion containing transistors of a second conductivity type, said first and second circuit portions being interconnected and the interconnection defining an output, said first circuit portion being responsive to first and second complementary pulse signals and first dc bias signal, said second circuit portion being responsive to third and fourth complementary pulse signals and a second dc bias signal.

21. A processor system according as in claim 20 further comprising a respective capacitor circuit for coupling said second and fourth complementary signals to said respective first and second circuit portions.

22. A processor system comprising:

a processor; and

a data device coupled to said processor, at least one of said processor and data device including a charge pump circuit, said charge pump circuit comprising:

a p-channel switching transistor, said p-channel switching transistor having a gate for receiving a first switching signal;

a p-channel bias transistor connected in series with said p-channel switching transistor, said p-channel bias transistor having a gate for receiving a bias voltage, said serially connected p-channel switching transistor and p-channel bias transistor being connected between a first potential source and an output terminal;

an n-channel switching transistor, said n-channel switching transistor having a gate for receiving a second switching signal;

an n-channel bias transistor connected in series with said n-channel switching transistor, said n-channel bias transistor having a gate for receiving a bias voltage, said serially connected n-channel switching

transistor and n-channel bias transistor being connected between said output terminal and a second potential source;

a first capacitor for coupling a complementary version of said first switching signal to a connection node of said p-channel transistors; and

a second capacitor for coupling a complementary version of said second switching signal to a connection node of said n-channel transistors.

23. A method of operating a charge pump comprising:

switching a first switching transistor in response to a first applied switching signal to affect an output at an output terminal;

switching a second switching transistor in response to a second applied switching signal to affect an output at said output terminal;

biasing the switching characteristics of said first and second switching transistors with bias transistors respectively serially connected to said first and second switching transistors;

coupling a complementary signal of said first applied switching signal to a connection between said first switching transistor and an associated bias transistor; and

coupling a complementary signal of said second applied switching signal to a connection between said second switching transistor and an associated bias transistor.

24. A method as in claim 23 wherein said coupling is a capacitive coupling.

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